Programme 24 October 2017

09.00 **Opening and welcome**

Jari Nurmi, Tampere University of Technology, FI
Atila Alvandpour, Linköping University, SE

1. Plenary session

Chair: Atila Alvandpour, Linköping University, SE

09.15 **Invited talk: 5G applications trends and technology needs**
Sven Mattisson, Ericsson AB, SE

10.00 A 45nm CMOS SOI, Four Element Phased Array Receiver Supporting Two MIMO Channels for 5G
Shaheen, Rana A.; Akbar, Rehman; Sethi, Alok; Aikio, Janne P.; Rahkonen, Timo; Pärssinen, Aarno, University of Oulu, FI

10.20 Can Real-Time Systems Benefit from Dynamic Partial Reconfiguration?
Pezzarossa, Luca; Toftegaard Kristensen, Andreas; Schoeberl, Martin; Sparsø, Jens, Technical University of Denmark, DK

10.40 **Coffee break**

	2.1 RF Receivers Chair: Kari Halonen, Aalto University, FI	2.2 Processing Architectures Chair: Johnny Öberg, Royal Institute of Technology, SE
11.10	A Fully Integrated 13 GHz CMOS SOI stacked Power Amplifier for 5G Wireless Systems *Aikio, Janne P.; Sethi, Alok; Shaheen, Rana A.; Akbar, Rehman; Rahkonen, Timo; Pärssinen, Aarno, University of Oulu, FI*	A Shared Scratchpad Memory with Synchronization Support *Hansen, Henrik Enggaard; Maroun, Emad Jacob; Kristensen, Andreas Toftegaard; Marquart, Jimmi; Schoeberl, Martin, Technical University of Denmark, DK*
11.30	A highly compact, 16.8 dBm Psat Ka-band Power Amplifier in 250 nm SiGeC BiCMOS *Somesanu, Iancu; Schumacher, Hermann, Ulm University, DE*	Improving Microarchitecture Design and Hardware Generation using Micro-Language IP Cores *Antonov, Alexander Alexandrovich; Kustarev, Pavel Valerievich; Bikovsky, Sergey Vyacheslavovich, ITMO University, RU*
11.50	Digital centric IF-DAC based Heterodyne Transmitter Architecture *Hanay, Oner; Bayram, Erkan; Negra, Renato, RWTH Aachen University, DE*	Supporting Concurrent Memory Access in TCF-aware Processor Architectures *Forsell, Martti; Roivainen, Jussi; Leppänen, Ville; Träff, Jesper Larsson, VTT, FI*
12.10	The effect of DPD bandwidth limitation on EVM for a 28 nm WLAN 802.11ac transmitter *Morales Chacón, Oscar; Johansson, Ted; Flink, Thomas, Linköping University, SE*	Power Mitigation of a Heterogeneous Multicore Architecture by Frequency Scaling in an OFDM Receiver Test Case *Nouri, Sajjad; Nurmi, Jari, Tampere University of Technology, FI*

12.30 **Lunch**

3.1 RF Receivers

Chair: Henrik Sjöland, Lund University, SE

13.40 Design of High-Performance E-band SPDT Switch and LNA in 0.13 µm SiGe BiCMOS Technology
Ahamed, Raju; Varonen, Mikko; Parveg, Dristy; Saijets, Jan; Halonen, Kari A. I., Aalto University, FI

14.00 Subsampling Phase-Locked Loop Behavioural Modelling Approach for Phase Noise Evaluation
Gjurovski, Peco; Wei, Muh-Dey; Negra, Renato, RWTH Aachen University, DE

14.20 A Self-consistent Carleman Linearization Approach for the Design of RF Mixer Circuits
Weber, Harry; Koroa, Gerald Alexander; Delchev, Dimitar; Marinova, Galia; Mathis, Wolfgang, Leibniz Universität Hannover, DE

3.2 Emerging Technologies

Chair: Peeter Ellervee, Tallinn University of Technology, EE

A Dependable ASIC Architecture with RT-level Rollback for Controller Soft Error Recovery
Inoue, Keisuke, Kanazawa Technical College, JP

A Call-up for Circuit-Switched NoCs in the Dark-Silicon Era
Naguib, Salma Hesham[1,2]; Goehringer, Diana[3]; Abd El Ghany, Mohamed A.[1,4], 1: German University in Cairo, EG; 2: Ruhr-University Bochum, DE; 3: TU Dresden, DE; 4: TU Darmstadt, DE

Designing A Differential 3R-2Bit RRAM Cell for Enhancing Read Margin in Crosspoint RRAM Arrays
Nakhkash, Mohammad Reza; Bardareh, Hossein; Zokaee, Farzaneh; Zarandi, Hamid Reza, Amirkabir University of Technology Tehran Polytechnique, IR

4. Poster session I

Coffee break

14.40 A Capacitance Multiplier Based on DBTA
Vavra, Jiri, University of Defence, CZ

Bi-static environmental SAR radar imager
Eriksrød, J. Håvard H.; Kjelgård, Kristian G.; Tømmer, Mathias; Burkhart, John F.; Lande, T.S., University of Oslo, NO

Zero-Crossing Detector for a Piezoelectric Energy Harvester
Schüffny, Franz Marcus; Hayoz, Michel; Bae, Cheolyong; Arya, Ishan; Gokhale, Madhur; Hema Chandar, Annapragada; Nielsen, Linköping University, SE

Implementation of a Fault-Tolerant, Globally-Asynchronous-Locally-Synchronous, Inter-Chip NoC Communication Bridge on FPGAs
Kyriakakis, Eleftherios; Ngo, Kalle; Öberg, Johnny, KTH Royal Institute of Technology, SE

Analysis of a high-speed PCB design
Johansson, Christian, Månefjord, Torbjörn, Saab AB, SE

A High-Resolution Reconfigurable Sigma-Delta Digital-to-Analog Converter for RF Pulse Transmission in MRI Scanners
Qazi, Sohaib Ayaz[1]; Ali Shah, Syed Asmat[2]; Omer, Hammad[1]; Wikner, Jacob[3], 1: COMSATS Institute of Information Technology, PK, 2: Chungbuk National University, KR, 3: Linköping University, SE

15.30 **Invited talk: Massive MIMO is one the key technologies for 5G and beyond**
Erik G. Larsson, Linköping University, SE

5.1 RF Transmitters

Chair: Ted Johansson, Linköping University, SE

16.15 Design and Analysis of High Performance Pulse Ring VCO
Dalakoti, Aditya; Miller, Merritt; Brewer, Forrest, University of California Santa Barbara, USA

16.35 A 1.8mW 450-900MHz ±15ps period jitter programmable multi-output clock generator with high supply noise tolerance in 28-nm CMOS process
Odedara, Bhavin[1]; Bojja, Srikanth[1]; Gupta, Nitin[1]; Rapoport, Igor; Ross, Tony[3]; Zelichenok, Alik, 1: Western Digital, IN; 2: Western Digital, IL; 3: Western Digital, USA

16.55 A 10-bit Active RF Phase Shifter for 5G Wireless Systems
Sethi, Alok; Aikio, Janne P.; Shaheen, Rana A.; Akbar, Rehman; Rahkonen, Timo; Pärssinen, Aarno, University of Oulu, FI

17.15 Break

19.00 **Dinner**

5.2 SoC Design

Chair: Jens Sparsø, Technical University of Denmark, DK

Workload Prediction for Runtime Resource Management
Niknafs, Mina; Ukhov, Ivan; Eles, Petru; Peng, Zebo, Linköping University, SE

Performance Estimation of Embedded Applications on Microcontrollers
Ruberg, Priit; Lass, Keijo; Liiv, Elvar; Ellervee, Peeter, Tallinn University of Technology, EE

Exploration of FPGA Architectures for Tight Coupled Accelerators in a 22nm FDSOI Technology
Bauer, Heiner; Höppner, Sebastian; Partzsch, Johannes; Walter, Dennis; Mayr, Christian; Schraut, Florian; Eisenreich, Technische Universität Dresden, DE

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09.00 **Invited talk: Run-time task mapping on multicore architectures**
André Kokkeler, University of Twente, NL

6. Poster session II

Coffee break

09.45 Single Event Upset Detector Based on COTS FPGA
Ngo, Kalle; Mohammadat, Tage; Öberg, Johnny, KTH Royal Institute of Technology, SE

Power Efficiency optimization of Charge Pumps in Embedded Low voltage NOR Flash Memory
Ngueya Wandji, Steve; Portal, Jean-Michel; Aziza, Hassen; Mellier, Julien; Ricard, Stephane, IM2NP UMR 7334 Aix Marseille University, FR

High Level Synthesis for Reduction of WCET in Real-Time Systems
Kristensen, Andreas Toftegaard; Pezzarossa, Luca; Sparsø, Jens, Technical University of Denmark, DK

An RNS Based Modular Multiplier with Reduced Complexity
Asif, Shahzad[1]; Vesterbacka, Mark[2], 1: Western Sydney University, AU and 2: Linköping University, SE

Towards Software Performance Estimation based on Register-Transfer Level Descriptions
Puttnies, Henning; Christoph, Niemann; Sascha, Rohde; Dirk, Timmermann; Jörg, Schacht, University of Rostock, DE

Variable-Accuracy Bit-serial Multiplication with Row Bypassing for Ultra Low Power
Lu, Yue; Kazmierski, Tom, University of Southampton, UK

6.1 Power Electronics and Energy Harvesting

Chair: Atila Alvandpour, Linköping University, SE

10.30 Synthesis and Design of a Fully Integrated Multi-Topology Switched Capacitor DC-DC Converter with Gearbox Control
Davidsen, Jeppe Gaardsted; Yosef-Hay, Yoni; Larsen, Dennis Øland; Jørgensen, Ivan H. H., Technical University of Denmark, DK

10.50 Active Charge Pumping Power-saving Technique for SC Integrators
sun, jia; Rahkonen, Timo, University of Oulu, FI

11.10 Ring-oscillator-based timing generator for ultralow-power applications

6.2 DSP Hardware

Chair: Mark Vesterbacka, Linköping University, SE

Unrolled Layered Architectures for Non-Surjective Finite Alphabet Iterative Decoders
Boncalo, Oana[1]; Savin, Valentin[2]; Amaricai, Alexandru[1], 1: University Politehnica Timisoara, RO, 2: CEA-LETI, FR

Design and Implementation of a Multi-mode Harris corner Detector Architecture
Li, Jingui[2]; Viitanen, Timo[2]; Li, Lin[1]; Takala, Jarmo[2]; Bhattacharyya, Shuvra[1,2], 1: University of Maryland, USA, 2: Tampere University of Technology, FI

Implementation of a Performance Optimized Database Join Operation on FPGA-GPU Platforms Using OpenCL,

	Angelov, Pavel; Nielsen-Lönn, Martin; Alvandpour, Atila, Linköping University, SE	*Roozmeh, Mehdi; Lavagno, Luciano, Politecnico di Torino, IT*
11.30	Self-oscillating multilevel switched-capacitor DC/DC converter for energy harvesting *Nielsen-Lönn, Martin; Angelov, Pavel; Wikner, J Jacob; Alvandpour, Atila, Linköping University, SE*	Hands-free system using stereo noise suppression method for automatic driving *Takasawa, Nobuaki; Natori, Takahiro; Tanabe, Nari; Furukawa, Toshihiro, Tokyo University of Science, Suwa, JP*
11.50	**Lunch**	

7. Plenary Session

Chair: Jari Nurmi, Tampere University of Technology, FI

13.00 **Invited talk: Accelerating Datacenter Workloads**
Enno Luebbers, Intel, USA

13.45 Dependability Evaluation of SISO Control-Theoretic Power Managers for Processor Architectures
Shahosseini, Sina; Moazzemi, Kasra; Rahmani, Amir M.; Dutt, Nikil, UC Irvine USA, and TU Wien, AT

14.05 A Single Chip 16 GS/s Arbitrary Waveform Generator in 0.13 µm BiCMOS Technology
Ostrovsky, P.; Tittelbach-Helmrich, K.; Herzel, F.; Schrape, O.; Fischer, G.; Kissinger, D.; Börner, P.; Loose, IHP GmbH, DE

14.25 NorCAS 2018 announcement and Best Paper Award

14.30 Coffee

	8.1 Biomedical Chair: Jacob Wikner, Linköping University, SE	8.2 Dependability Chair: Peeter Ellervee, Tallinn University of Technology, EE
15.00	Three-Dimensional Millimeter-wave Frequency-shift-based CMOS Biosensor Using Vertically Stacked LC Oscillators *Matsunaga, Maya; Nakanishi, Taiki; Kobayashi, Atsuki; Nakazato, Kazuo; Niitsu, Kiichi, Nagoya University, JP*	ESD Induced EMS Problems in Digital IOs *Ostermann, Timm, Johannes Kepler University of Linz, AT*
15.20	High-Voltage Integrated Linear Regulator with Current Sinking Capabilities for Portable Ultrasound Scanner *Vendrell, Guifré; Llimós, Pere; Jørgensen, Ivan H. H., Technical University of Denmark, DK*	CMOS Digital Design of a Trusted Virtual Sensor *Martinez-Rodriguez, Macarena Cristina; Prada, Miguel Angel; Brox, Piedad; Baturone, Iluminada, IMSE, CNM, CSIC, Universidad de Sevilla, ES*
15.40	Energy-Efficient Neuromorphic Receptors for Wide-Range Temporal Patterns of Post-Synaptic Response *You, Xuefei; Zjajo, Amir; Kumar, Sumeet S.; van Leuken, Rene, Delft University of Technology, NL*	Mitigating Single-Event Upsets in COTS SDRAM using an EDAC SDRAM Controller *Kyriakakis, Eleftherios; Ngo, Kalle; Öberg, Johnny, KTH Royal Institute of Technology, SE*
16.00	Finish	